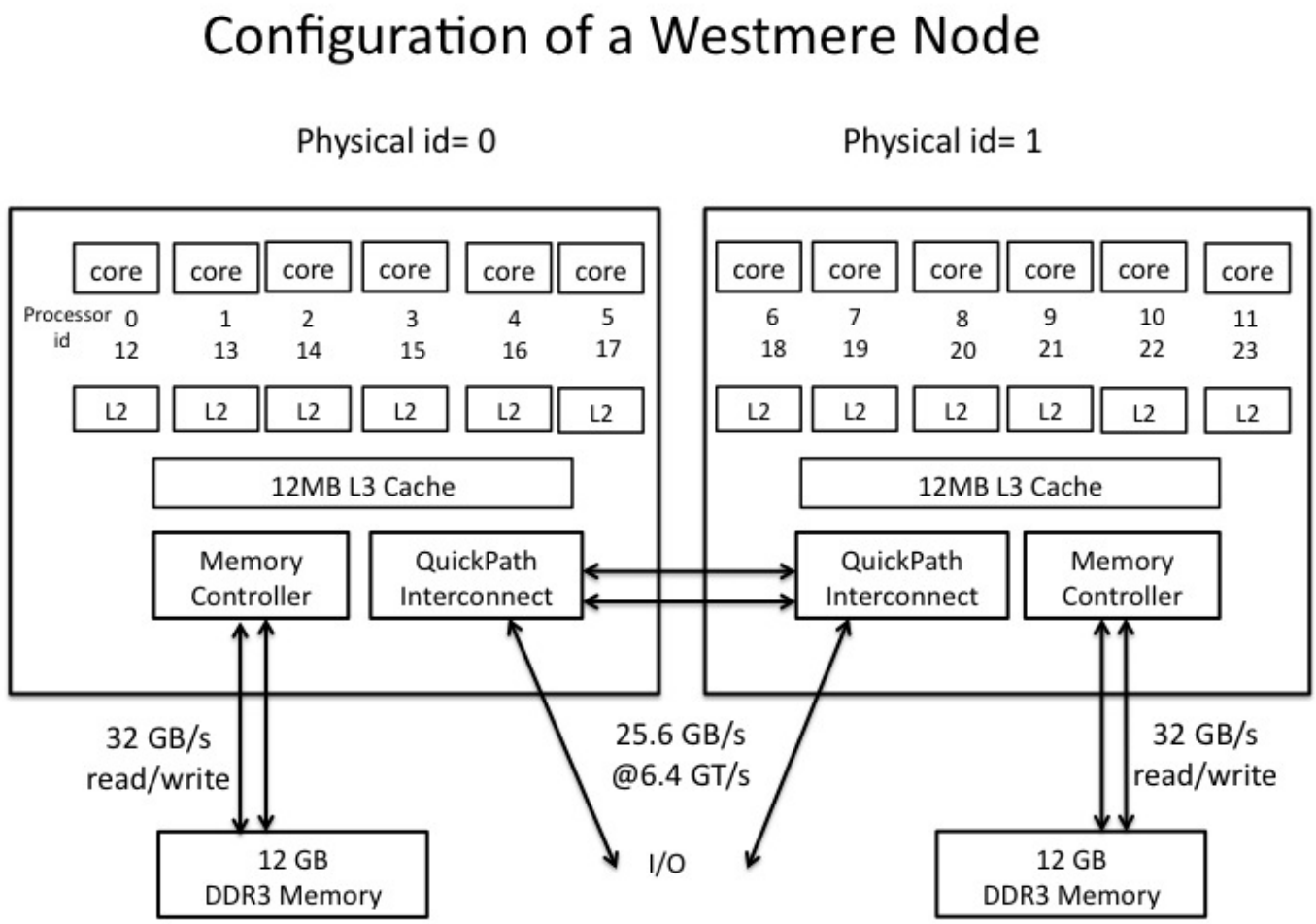
Westmere Processors

Category: Pleiades

DRAFT

This article is being reviewed for completeness and technical accuracy.

Configuration of a Westmere node:



Core Labeling:

Unlike Harpertown, the core labeling in Westmere is contiguous. That is, cores 0-5 are in first socket and cores 6-11 are in the second socket.

When using the SGI MPT library, the enviroment variable **MPI_DSM_DISTRIBUTE** is set to *on* by default for the Westmere nodes.

SSE4 Instruction Set:

Intel's Streaming SIMD Extensions 4.2 (SSE4.2) instruction set is included in the Westmere processors.

Since the instruction set is upward compatible, an application that is compiled with -xSSE4.1 (with Intel version 11 compiler) can run on either Harpertown or Nehalem-EP or Westmere processors. An application that is compiled with -xSSE4.2 can run ONLY on Nehalem-EP or Westmere processors.

If you wish to have a single executable that will run on any of the three Pleiades processor types with suitable optimization to be determined at run time, you can compile your application with -O3 -ipo -axSSE4.2,xSSE4.1

Hyperthreading:

Hyperthreading is available by user request on the Westmere nodes (for example, by asking for more than 12 ranks per node).

Turbo Boost:

Turbo Boost is set to *ON* on the Westmere nodes.

Article ID: 80
Last updated: 27 Oct, 2011
Computing at NAS -> Computing Hardware -> Pleiades -> Westmere Processors
http://www.nas.nasa.gov/hecc/support/kb/entry/80/?ajax=1